METHOD AND DEVICE FOR GENERATING A SIGNAL WITH A FREQUENCY EQUAL TO THE PRODUCT OF A REFERENCE FREQUENCY AND A REAL NUMBER

Field of the Invention

[0001]   The invention relates to frequency synthesis and is advantageous, but not limited, to wireless communication, and in particular, to mobile telephones that incorporate frequency synthesis within their transmission/reception system.

Background of the Invention

[0002]   A phase locked loop (PLL) is widely used for frequency synthesis. This type of looped system can multiply a reference frequency by an integer number and thus address an entire frequency range at a certain frequency step. More precisely, a phase locked loop is a servo-control system generating a frequency N times greater than the reference frequency that it receives in input, where N is an integer number. Thus, the output frequency given by a voltage-controlled oscillator is divided by N, and is then compared with a reference that may be supplied by a quartz. A charge pump formed from two current sources then reacts by injecting current into or drawing current out of the integrator filter that controls the output oscillator.

[0003]   If the oscillator output frequency is an increasing function of its input voltage, the loop

reaction is based on the following principle. The front comparator detects the first of the two fronts or leading edges. If this detected front belongs to the reference signal, the charge pump receives the command to send the current into the integrator filter. In this case, the output signal divided by N is delayed from the reference signal, and therefore the voltage at the oscillator terminals has to be increased.

[0004] Conversely, if the first detected front is the front of the output signal divided by N, the charge pump absorbs the current so that the voltage at the oscillator terminals drop. When the second front appears, the charge pump stops its activity while waiting for the next front. Thus, as the fronts become closer, the injected charge will be lower until the frequency of the oscillator output signal converges towards N times the reference frequency.

[0005] The phase locked loops can be used to synthesize frequencies with high precision and good stability. Their limitation is due to the fact that it is only possible to synthesize multiple integers, which limits the number of frequencies that can be addressed from a single reference frequency.

[0006] In order to overcome the problem of non-integer division, a "fractional" phase locked loop can be used that performs a succession of divisions by N and N+1. Thus, to make a division by N+0.5, we will divide once by N, then by N+1, and so on. The loop integrator filter then averages the value of the voltage controlling the loop output oscillator.

[0007] This type of architecture is one approach for dividing with a decimal part, but it introduces severe noise problems. Unlike the conventional phase locked

loops mentioned above in which current injections are reduced until they become negligible under steady state conditions, fractional phase locked loops require large current injections at all times during their operation, since the frequency is between N and N+1 times the reference frequency, and it can only be compared at integer divisions.

[0008]   These repeated current injections create noise that must be distributed. The size of the binary sequence controlling the divider by N or N+1 will impose this distribution. When the sequence is minimum, the oscillator voltage is modulated at the communication frequency of the dividers by N and N+1. The loop output spectrum then comprises two parasitic spikes. These spikes may cause major problems if they do respect noise specifications around the fundamental.

[0009]   Furthermore, when the sequence becomes larger, parasite spikes due to the period of the sequence tend to spread. However, the loop integrator filter then has the time to react, which results in a variation of the fundamental with time. Thus, for very long sequences, parasitic spikes can be treated like noise distributed around the generated frequency, as a result of unwanted modulation of the output frequency.

[0010]   In conclusion, the stability of the output frequency and the noise minimum very much limit the use of fractional phase locked loops.

Summary of the Invention

[0011]   One purpose of the invention is to propose a frequency synthesis that keeps all the advantages of conventional phase locked loops while eliminating noise inherent to fractional phase locked loops. Therefore,

the invention proposes a method for generating a required signal with a required frequency equal to the product of a reference frequency and a real number.

[0012]   According to one general characteristic of the invention, the method cyclically comprises a sequence of measurement phases and correction phases. The measurement phase may comprise a first integer division of the frequency of an oscillator output signal by a first integer divider so as to obtain a first intermediate signal. A first measurement signal representative of the time difference between this first intermediate signal and a reference signal according to the reference frequency is then determined.

[0013]   A first comparison signal derived from the first measurement signal is then compared with a second comparison signal that depends on the reference period, the integer part and the decimal part of the real number, and the first integer divider so as to obtain an error signal representative of the time difference between the period of the current output signal from the oscillator and the required period.

[0014]   The correction phase may comprise a deactivation of the first frequency divider and a correction of the oscillator control starting from the error signal. The oscillator output signal forms the required signal.

[0015]   In other words, in general, the measurement phase takes place at least using a time deviation measurement loop with an integer division. This loop is open on the input side of the voltage controlled oscillator. Thus, during a measurement period which may for example be a period of the reference signal,

the first comparison signal which may for example be equal to the product of the first measurement signal and a weighting factor, is compared with a second comparison signal which, when a single loop is used, is similar to a set signal. The set signal represents the time difference between the reference signal and a signal for which the period is equal to N1 times the required period of the required output signal, where N1 is the first integer divider.

[0016]   The invention thus provides precise information about the difference between the output frequency and the required frequency, and the loop reacts to the real deviation such that the loop becomes stable and there are no parasitic spikes inherent to conventional fractional phase locked loops.

[0017]   When the measurement phase is made during one reference signal period, the correction phase can then take place during the next period of the reference signal, and so on. The measurement phase may more generally take place during an integer number of periods of the reference signal while the correction phase may take place during another integer number of subsequent periods of the reference signal, identical to or different from the first integer number.

[0018]   According to one preferred embodiment of the invention, the second comparison signal may be generated within a second time difference measurement loop with integer division. More precisely, according to this embodiment, generation of the second comparison signal may comprise a second integer division of the oscillator output signal frequency by a second integer divider so as to obtain a second intermediate signal. Determination of a second measurement signal

representative of the time difference between this second intermediate signal and the reference signal is made. The second intermediate signal is weighted by a second weighting factor obtained from the first integer divider, the integer part and the decimal part of the real number.

[0019]   Furthermore, generation of the first comparison signal includes weighting of the first measurement signal by a first weighting factor obtained from the second integer divider, the integer part and the decimal part of the real number.

[0020]   The correction phase then also comprises deactivation of the second frequency divider. Thus, for example, if the first integer divider is equal to N1 and the second integer divider is equal to N2, the first weighting factor may be equal to $-(N2-N-f)$ while the second weighting factor will be equal to $N1-N-f$. The variables N and f denote the integer part and the decimal part respectively of the real number which when multiplied by the reference frequency supplies the required frequency.

[0021]   One particular straightforward way of implementing the invention includes for example using a first integer divider equal to $N+1$ and a second integer divider equal to $N-1$. The first weighting factor is then equal to $1+f$ while the second weighting factor is then equal to $1-f$.

[0022]   Another purpose of the invention is to provide a device for generation of a required signal with a required frequency equal to the product of a reference frequency and a real number.

[0023]   According to one general characteristic of the invention, the device may comprise a controlled

oscillator, and first division means capable of making a first integer division of the oscillator output signal frequency by a first integer divider so as to obtain a first intermediate signal. First determination means are capable of determining a first measurement signal representative of the time difference between this first intermediate signal and a reference signal with the reference frequency.

[0024] The device may further comprise generation means capable of generating a first comparison signal derived from the first measurement signal, and second generation means capable of generating a second comparison signal dependent on the reference period, the integer part and the decimal part of the real number and the first integer divider.

[0025] Comparison means are capable of making a comparison between the two comparison signals so as to obtain an error signal representative of the time difference between the period of the current output signal from the oscillator and the required period. A switch is connected between the output from the comparison means and the oscillator control input.

[0026] Control means open and close the switch successively and cyclically and deactivating the first divider when the switch is closed, so as to successively enable determination of the error signal and to deliver this error signal on the oscillator control input. The oscillator output signal forms the required signal. According to one embodiment of the invention, the control means open and then close the switch during successive periods of the reference signal.

[0027] According to one advantageous embodiment of

the invention, the second generation means may comprise a second divider capable of making a second integer division of the oscillator output signal frequency, and second determination means capable of determining a second measurement signal representative of the time difference between this second intermediate signal and the reference signal. Second weighting means are capable of weighting the second intermediate signal by a second weighting factor obtained from the first integer divider, the integer part and the decimal part of the real number.

[0028]   Furthermore, according to this embodiment, the first generation means may comprise first weighting means capable of weighting the first measurement signal by a weighting factor obtained from the second integer divider, the integer part and the decimal part of the real number. The control means may also be designed to deactivate the second divider when the switch is closed.

[0029]   The device according to the invention is advantageously made in the form of an integrated circuit. The invention is also applicable to a terminal of a wireless communication system comprising a generation device as defined above. For example, this terminal could be a mobile cell phone.

Brief Description of the Drawings

[0030]   Other advantages and characteristics of the invention will become clear after reading the detailed description of one embodiment and usage method, which is in no way to be limiting, and the appended drawings, wherein:

[0031]   Figure 1 diagrammatically illustrates a

mobile cell phone incorporating a device according to the present invention; and

[0032]   Figure 2 diagrammatically illustrates in more detail one embodiment of the device according to the present invention.

Detailed Description of the Preferred Embodiments

[0033]   In Figure 1, the reference TP denotes a remote terminal, like a mobile cell phone, that is in communication with a base station BS1, for example using a CDMA-FDD type communication system. The mobile cell phone conventionally comprises an analog radio frequency stage ERF connected to an antenna ANT to receive an input signal ISG.

[0034]   Conventionally, the ERF stage comprises a low noise amplifier LNA and two processing channels comprising mixers, filters and conventional amplifiers (not shown in Figure 1). Both of the two mixers receive two signals OL from a device FFLL, with a phase difference between them of 90°. After frequency transposition in the mixers, the two processing channels define two flows, I (direct flow) and Q (flow in quadrature), to use terminology well known to those skilled in the art.

[0035]   After digital conversion in the analog/digital converters, the two I and Q flows are output to a reception processing stage ETNR. This processing stage ETNR comprises a receiver RR, commonly referred to as a Rake receiver, followed by conventional demodulation means MP that demodulate the frequency spectrum output by the Rake receiver RR. The demodulation means MP are followed by a conventional channel decoder CD.

[0036] We will now refer more particularly to Figure 2 to illustrate one embodiment of a frequency tuner device FFLL according to the invention. This device comprises a voltage-controlled oscillator VCO, for which the output delivers the required output signal, in fact the local oscillator signal OL (Figure 1). Obviously, the phase shift between the two local oscillator signals OL illustrated in Figure 1 can easily be obtained by placing a phase shifter at the output from the oscillator VCO. Although a voltage controlled oscillator is shown in this case, any type of controlled oscillator will be suitable, for example a current controlled oscillator.

[0037] In this case, the device FFLL comprises two loops B1 and B2. The first loop B1 comprises a first divider DV1 capable of making an integer division, in fact by N, of the output signal delivered by the oscillator VCO. This first intermediate signal SI1 delivered by the divider DV1 is supplied to the first determination means CP1, in this case comprising a front detector followed by a charge pump. These first determination means CP1 also receive a reference signal SRF with a reference period T_{ref}. This reference signal SRF is output by a quartz QTZ.

[0038] A first capacitor C1 is also connected between ground and the output from the first determination means CP1. Moreover, the first weighting means PPD1 are connected between the other terminal of the capacitance of capacitor C1 and the first input of a subtractor CMP (comparison means).

[0039] The output from the subtractor is connected to the filter of loop K through a switch A controlled at the reference frequency F_{ref} by a control signal SW

output by the control means MCM. The output from the loop filter K is connected to the oscillator VCO and to a capacitor C_{vcq} to control the control voltage of the oscillator.

[0040] The second loop B2 of the device FFLL comprises a second divider DV2 that can also make an integer division of the output signal from the oscillator VCO. This second divider actually divides by N-1 and outputs a second intermediate signal SI2 to the second determination means CP2 with a structure similar to the first determination means CP1.

[0041] These second determination means also receive the reference signal SRF. A second capacitor C2 is connected to the output from means CP2 and to the second weighting means PPD2. The output from these second weighting means PPD2 is connected to the other input of the subtractor CMP.

[0042] Furthermore, the two dividers DV1 and DV2 may be activated or deactivated respectively by two logical signals DS1, DS2 also output by the control means MCM. The device according to the invention can thus directly make a division by a real number with a decimal part with several bits, actually by a number equal to N+f where N denotes the integer part of the real divider and f denotes the decimal part. Therefore the invention differs from the prior art, and particularly from fractional phase locked systems that require the alternate use of two integer divisions.

[0043] According to the embodiment shown in Figure 2, the integer divisions by N+1 and by N-1 are made simultaneously, so that the difference between the output frequency and the required frequency is known exactly. Thus, the loops react to the real difference

and not to the difference between the output frequency and an integer number times the reference. The difference reduces until it becomes negligible. The loop remains stable and parasitic spikes inherent to conventional fractional phase locked loops disappear.

[0044] More precisely, the method according to the invention is spread over two phases, namely a measurement phase and a correction phase. The measurement phase is made on one measurement period, for example a reference signal period S_{ref}.

[0045] This measurement period is used to measure the output frequency F_{out}. During this time, the set of two loops B1 and B2 is open at switch A, immediately before capacitor C_{vco} maintaining the oscillator control voltage, to prevent the loop reaction from disturbing the measurement. Loop B2 measures the time difference between the second intermediate signal SI2 with a period equal to $(N-1)T_{out}$ and the reference signal with period T_{ref}.

[0046] At the end of the measurement, the voltage at the terminals of capacitor C2 is equal to

$$V_2 = \frac{I_0}{C_2}\left[T_{ref} - (N-1)T_{out}\right] \quad (I)$$

Loop B1 supplies the difference between the first intermediate signal SI1 with a period equal to $(N+1)T_{out}$ and the reference signal.

[0047] At the end of the measurement, the voltage at the terminals of the capacitor C1 is equal to:

$$V_1 = \frac{I_0}{C_2}\left[(N+1)T_{out} - T_{ref}\right] \quad (II)$$

The correction phase is then carried out during the next period after the reference signal. The frequency dividers DV1 and DV2 are deactivated and reset to 0 and switch A is closed. The voltages of the two capacitors weighted by factors equal to (1+f) and (1-f) are then subtracted. The voltage V obtained gives the difference between the output frequency and the required frequency.

[0048]   This voltage is supplied by formula (III) below

$$V = (1+f)\frac{I_0}{C_1}\Big[(N+1)T_{out} - T_{ref}\Big] - (1-f)\frac{I_0}{C_2}\Big[T_{ref} - (N-1)T_{out}\Big] \quad (III)$$

If C1 = C2 = C$_0$, the voltage V is given by the following formula which then reduces to formula (IV)

$$V =$$

$$\frac{I_0}{C_0}\Big\lfloor(N+1)T_{out} - T_{ref} + (N-1)T_{out} - T_{ref} + f\big[(N+1)T_{out} - T_{ref} + T_{ref} - (N-1)T_{out}\big]\Big\rfloor$$

$$V = \frac{2.I_0}{C_0}\Big[(N+f)T_{out} - T_{ref}\Big] \quad (IV)$$

Therefore, the difference between the required period and the actual period is available.

[0049]   This voltage is then transformed to a current so that it can be integrated in the capacitor C_{vco}. The capacitances of the charge pumps have to be drained before starting the measurement again. In other words, during an integer number of subsequent periods of the reference signal (for example, during the next period).

The counters will be activated at the next front of the reference signal.

[0050]   Thus, the system according to the invention is capable of multiplying the frequency by a real number with a decimal part, and maintains all the advantages of conventional phase locked loops while eliminating noise inherent to fractional phase locked loops.